APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/760,431	01/20/2004	Duane Arlyn Averill	ROC920030390US1	9190

7590 06/16/2006	EXAMINER
Robert R. Williams	CHERY, MARDOCHEE
IBM Corporation, Dept. 917	

	ART UNIT	PAPER NUMBER
3605 Highway 52 North	2188	
Rochester, MN 55901-7829		

DATE MAILED: 06/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	10/760,431	AVERILL ET AL.
	Examiner	Art Unit	
	Mardochee Chery	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2004*.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

   4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   a)☐ All b)☐ Some * c)☐ None of:

   1.☐ Certified copies of the priority documents have been received.

   2.☐ Certified copies of the priority documents have been received in Application No. _____.

   3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
   Paper No(s)/Mail Date *1/20/04*.

4) ☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2.   Claims 1, 2, 5-8 are rejected under 35 U.S.C. 102(b) as being anticipated by

Baumgartner (6,108,764).

As per claim 1, Baumgatner discloses a digital data processing system,

comprising: a memory [Fig. 1; *memory 18*]; at least one processor having at least one

associated cache for temporarily caching data from said memory [Fig. 1; *processor 12;*

cache 14]; at least one device having a device cache, said device cache having a fixed

number of slots for caching data, each slot caching a cache line of data [Fig. 1; *10a-10m*];

and a cache coherency mechanism, said cache coherency mechanism including a

cache line state directory structure, said cache coherency mechanism selectively

determining whether to send cache line invalidation messages to said at least one

device using state information in said cache line state directory structure, wherein at

least a portion of said cache line state directory structure contains a plurality of cache

line entries, each entry corresponding to a respective one of said plurality of slots for

caching data of said device cache [Fig. 2; *Directory control logic 58; Coherency Response Logic*

56; Transaction Send Unit (TSU); Data Send Unit (DSU); Transaction Receive Unit (TRU); Data Receive

Unit (DRU); Table V, Table VI].

As per claim 2, Baumgatner discloses wherein said device is an I/O bridge device [Fig. 1; I/O devices 32 and Mezzanine bus 30].

As per claim 5, Baumgartner discloses said digital data processing system comprises a plurality of nodes, each node containing at least one processor, a respective portion of said memory, and a respective portion of said cache coherency mechanism [Fig. 3A].

As per claim 6, Baumgartner discloses each said respective portion of said cache coherency mechanism in each respective node maintains cache line state information for cached data having a real address in the respective portion of said memory contained in the node [Fig. 3B].

As per claim 7, Baumgartner discloses wherein each said respective portion of said cache coherency mechanism in each respective node maintains cache line state information for data cached in devices contained in the node [Fig. 3B].

As per claim 8, Baumgartner discloses wherein said digital data processing system comprises a plurality of devices having respective device caches, each said device cache having a respective fixed number of slots for caching data, each slot caching a cache line of data [Fig. 1]; and wherein said cache line state directory

structure includes a plurality of portions, each portion corresponding to a respective one of said plurality of devices, each portion containing a plurality of cache line entries, each entry corresponding to a respective one of said plurality of slots for caching data of the device cache to which the respective portion corresponds [Fig. 2].

Claim Rejections - 35 USC § 103

3.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4.   Claims 3-4, 9-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baumgartner (6,108,764) as applied to claim 1 above, and further in view of Carpenter (6,115,804).

As per claim 3, Baumgatner discloses wherein a processor portion of said cache line state directory structure contains cache line state for at least one said cache associated with a processor, [col. 7, ll 59-67].

However, Baumgartner does not specifically teach said cache coherency mechanism further selectively determining whether to send cache line invalidation messages to the processor with which the cache is associated using state information in said processor portion of said cache line directory structure as required.

Carpenter discloses said cache coherency mechanism further selectively determining whether to send cache line invalidation messages to the processor with which the cache is associated using state information in said processor portion of said cache line directory structure [col. 12, ll 1-34] to concurrently store an unmodified copy of a particular cache line in a recent coherency state from which the copy of the particular cache line can be sourced by shared intervention (col. 3, ll 1-5).

Since the technology for implementing a computer system having multiple caches with sending cache line invalidation messages to the processor with which the cache is associated using state information in said processor portion of said cache line directory structure was well know as evidenced by Carpenter, an artisan would have been motivated to implement this feature in the system of Baumgartner in order to concurrently store an unmodified copy of a particular cache line in a recent coherency state from which the copy of the particular cache line can be sourced by shared intervention. Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Baumgartner to include sending cache line invalidation messages to the processor with which the cache is associated using state information in said processor portion of said cache line directory structure because it was well known to concurrently store an unmodified copy of a particular cache line in a recent coherency state from which the copy of the particular cache line can be sourced by shared intervention (col. 3, ll 1-5) as taught by Carpenter.

As per claim 4, Carpenter discloses wherein said processor portion of said cache

line state directory structure contains cache line state for a plurality of caches

associated with a plurality of processors, said cache coherency mechanism further

selectively determining whether to send cache line invalidation messages to any of said

plurality of processors using state information in said processor portion of said cache

line directory structure [col. 11, ll 38-51].

As per claim 9, the rationale in the rejection of claims 3 and 8 is herein

incorporated.

As per claim 10, the rationale in the rejection of claim 2 is herein incorporated.

As per claim 11, Carpenter discloses receiving a plurality of data access requests

for cache lines of data from said device, each data access request from said device

including data identifying a slot of said device cache in which the cache line will be

stored [col. 11, ll 38-51]; and responsive to receiving each said data access request

from said device, updating said cache line state directory structure by writing cache line

identifying information corresponding to the data access request at the entry

corresponding to the slot in which the cache line requested by the data access request

will be stored [col. 12, ll 1-34].

As per claim 12, Carpenter discloses wherein said step of maintaining a cache

line state directory structure comprises maintaining a first portion of said cache line

state directory structure corresponding to said device cache, and a second portion of

said cache line state directory structure corresponding to a plurality of caches

associated with a plurality of processors, said method further comprising the steps of:

responsive to each of said plurality of data access requests, accessing said cache line

state directory structure to determine whether data having a data address referenced by

the request is contained in any of said plurality of processors [col. 11, ll 8-26]; for each

of said plurality of data access requests, determining whether to send an invalidation

message to any of said plurality of processors based on whether said step of accessing

said cache line state directory structure determines that data having a data address

referenced by the request is contained in any of said plurality of processors [col. 11, ll

38-51]; and for each of said plurality of data access requests, sending an invalidation

message to at least one of said plurality of processors responsive to the determination

made by said step of determining whether to send an invalidation message to any of

said plurality of processors [col. 12, ll 1-34].

As per claim 13, the rationale in the rejection of claim 5 is herein incorporated.

As per claim 14, the rationale in the rejection of claim 9 is herein incorporated.

As per claim 15, the rationale in the rejection of claim 2 is herein incorporated.

As per claim 16, the rationale in the rejection of claim 5 is herein incorporated.

As per claim 17, Carpenter discloses wherein each said respective portion of said cache line state directory structure each respective node contains cache line state information for cached data having a real address in the respective portion of said memory contained in the node [Fig. 2].

As per claim 18, Carpenter discloses wherein each said respective portion of said cache line state directory structure each respective node contains cache line state information for data cached in devices contained in the node [Fig. 3A].

As per claim 19, the rationale in the rejection of claim 9 is herein incorporated. Baumgartner further discloses a cache coherency apparatus for a digital data processing system: a communications interface for communicating with a plurality of devices [Fig. 1]; and cache coherence control logic which selectively generates invalidation messages responsive to events affecting the validity of cached data, said cache coherence control logic determining whether to send cache line invalidation messages to said first device using state information in said at least a portion of said cache line state directory structure corresponding to said cache in said first device [Fig. 2].

As per claim 20, the rationale in the rejection of claim 2 is herein incorporated.

As per claim 21, the rationale in the rejection of claim 3 is herein incorporated.

As per claim 22, Baumgartner discloses wherein said cache coherency apparatus is embodied in a single integrated circuit chip, said integrated circuit chip being separate from said first device [Fig. 2].

Conclusion

5.   When responding to the office action, Applicant is advised to clearly point out the patentable novelty that he or she thinks the claims present in view of the state of the art disclosed by references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111(c).

6.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mardochee Chery whose telephone number is (571) 272-4246. The examiner can normally be reached on 8:30A-5:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Manonama Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

June 12, 2006

Mardochee Chery
Examiner
AU 2188

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER